WHAT IS CLAIMED IS:

1. A synchronous switch for a telecommunications node, comprising:

a switch interface operable to terminate a bus and to receive from the bus a frame having a plurality of time slots that are each operable to transport a traffic cell;

a switch controller operable to determine a type for each traffic cell received at the switch interface and to determine based on the type for a traffic cell an address for storing the traffic cell in a switch memory; and

the switch memory operable to receive the traffic cell from the switch interface and the address for storing the traffic cell from the switch controller and to store the traffic cell at the address.

2. The synchronous switch of Claim 1, further comprising:

the switch interface operable to extract a header for the traffic cell from a time slot transporting the traffic cell and to provide the header to the switch controller; and

the switch controller further operable to determine the type for the traffic cell based on the header.

3. The synchronous switch of Claim 1, further comprising:

the switch memory comprising a plurality of time division multiplex (TDM) memory slots and a plurality of asynchronous transfer mode (ATM) queues associated with output ports; and

the switch controller further operable to determine an address of an ATM queue in the switch memory for storing a traffic cell in response to determining the traffic cell is of an ATM type and to determine an address of a TDM memory slot in the switch memory for storing a traffic cell in response to determining the traffic cell is of a TDM type.

4. The synchronous switch of Claim 3, further comprising:

the switch interface operable to extract a header for the traffic cell from a time slot transporting the traffic cell and to provide the header to the switch controller; and

the switch controller further operable to determine whether the traffic cell is of the ATM type or the TDM type based on the header.

5. The synchronous switch of Claim 1, wherein the switch interface, switch controller, and switch memory each operate at a synchronized frame pulse.

6. The synchronous switch of Claim 5, wherein the synchronized frame pulse is a 125 microsecond frame pulse.

7. The synchronous switch of Claim 1, further comprising the switch interface operable to terminate a plurality of point-to-point links of the bus and to receive from each link a frame having a plurality of the time slots.

8. The synchronous switch of Claim 7, wherein the point-to-point links of the bus operate at disparate rates.

9. The synchronous switch of Claim 1, wherein the traffic cell comprises an ATM cell.

10. The synchronous switch of Claim 1, further comprising:

the switch interface further operable to transmit on the bus an egress frame comprising a plurality of egress time slots that are each operable to transport a traffic cell;

the switch controller further operable to determine an address in the switch memory storing a traffic cell for transport in an egress time slot and to provide the address to the switch memory; and

the switch memory operable to write the traffic cell at the address in the switch memory to the egress time slot for transmission on the bus.

11. A switch card for a telecommunications node, comprising:

a switch interface operable to terminate a plurality of point-to-point links operating at disparate rates, to receive from each link a frame having a plurality of time slots that are each operable to transport a traffic cell, to extract a header for a traffic cell from the time slot transporting the traffic cell, and to provide the header to a switch controller;

the switch controller operable to determine a type for the traffic cell based on the header, to determine based on the type an address for storing the traffic cell in a switch memory, and to provide the address to the switch memory; and

the switch memory operable to receive the traffic cell from the switch interface and the address for storing the traffic cell from the switch controller, to associate the address with the traffic cell, and to store the traffic cell at the address.

12. The switch card of Claim 11, wherein the switch interface, switch controller, and switch memory each operate at a synchronized frame pulse.

13. The switch card of Claim 12, wherein the frame pulse comprises a 125 microsecond frame pulse.

14. The switch card of Claim 11, further comprising:

the switch interface further operable to transmit on each of the point-to-point links an egress frame comprising a plurality of egress time slots that are each operable to transport a traffic cell;

the switch controller further operable to determine an address in the switch memory storing a traffic cell to be transported in an egress time slot on a point-to-point link and to provide the address to the switch memory; and

the switch memory operable to write the traffic cell at the address in the switch memory to the egress time slot for transmission on the point-to-point link.

15. A method for switching traffic at a telecommunications node, comprising:

receiving a frame comprising a plurality of time slots each having a traffic cell and a header for the traffic cell;

determining a type for each traffic cell based on the header for the traffic cell;

determining an address in the switch memory for storing the traffic cell based on the type; and

storing the traffic cell in the switch memory at the address.

16. The method of Claim 15, further comprising:

receiving the frame at a switch interface;

extracting the header from the time slots at the switch interface;

passing the headers to a switch controller; and

determining the address at the switch controller based on the header.

17. The method of Claim 16, further comprising:

passing the traffic cell from the switch interface to the switch memory;

passing the address from the switch controller to the switch memory; and

associating the address with the traffic cell at the switch memory.

18. The method of Claim 17, further comprising operating the switch interface, switch controller, and switch memory at a synchronized frame pulse.

19. The method of Claim 15, wherein the switch memory comprises a plurality of time division multiplex (TDM) memory slots and a plurality of asynchronous transfer mode (ATM) queues associated with output ports, further comprising determining an address of an ATM queue in the switch memory for storing a traffic cell in response to determining the traffic cell is of an ATM type.

20. The method of Claim 19, further comprising determining an address of a TDM memory slot in the switch memory for storing a traffic cell in response to determining the traffic cell is of a TDM type.

21. The method of Claim 15, further comprising receiving a frame from each of a plurality of point-to-point links of a bus, each frame comprising a plurality of the time slots.

22. The method of Claim 15, further comprising:

transmitting an egress frame comprising a plurality of egress time slots that are each operable to transport a traffic cell;

determining an address in the switch memory storing a traffic cell for transport in an egress time slot; and

writing the traffic cell at the address in the switch memory to the egress time slot for transmission in the egress frame.

23. The method of Claim 16, further comprising:

the switch interface transmitting an egress frame comprising a plurality of egress time slots that are each operable to transport a traffic cell;

the switch controller determining an address in the switch memory storing a traffic cell for transport in an egress time slot and providing the address to the switch memory; and

the switch memory writing the traffic cell at the address in the switch memory to the egress time slot for transmission in the egress frame.

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